In the Claims:

1. (Currently Amended) A memory controller ~~An apparatus~~, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache ~~associated with~~ located on a memory module, the memory module coupled to the memory controller via a memory bus, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

2. Cancelled

3. (Currently Amended) The memory controller ~~The apparatus~~ of claim 1, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

4. (Currently Amended) The memory controller ~~The apparatus~~ of claim 3, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

5. (Currently Amended) The memory controller ~~The apparatus~~ of claim 4, each of the plurality of arrays of tag address storage locations organized into 4 ways.

6. (Currently Amended) A memory module ~~An apparatus~~, comprising:

a memory device; and

a data cache coupled to the memory device, the data cache controlled by commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

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7. Cancelled

8. (Currently Amended) The memory module ~~The apparatus~~ of claim 6, the data cache organized into a plurality of ways.

9. (Currently Amended) The memory module ~~The apparatus~~ of claim 8, the data cache organized into 4 ways.

10. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

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11. Cancelled

12. (Original) The system of claim 10, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

13. (Original) The system of claim 12, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

14. (Original) The system of claim 13, each of the plurality of arrays of tag address storage locations organized into 4 ways.

15. (Original) The system of claim 14, a point-to-point interconnect to couple the memory controller to the memory module.

Amendments to the Drawings

The attached sheet of drawings includes changes to Figure 5. Figure 5 has been amended to show a segmented cache line that is discussed in the specification and claimed in claim 1 but was not included in the original drawings.

Attachments: Replacement sheet

Annotated sheet showing changes to drawing